Abstract of the Disclosure

Disclosed is a processor clock generation circuit and related method for a low power consumption modem chip design, comprising a first clock generator for generating a first clock signal in response to enable and disable signals; a second clock generator for generating a second clock signal that is lower, in frequency, than the first clock signal; a decoder for decoding an externally inputted instruction to check whether the inputted instruction is a power-down instruction or a power-up instruction, and generating control signals; a clock selection unit for, if the instruction is the power-down instruction, outputting the second clock signal as a processor clock signal and outputting a clock change end signal in response to a control signal outputted from the decoder and, if the instruction is the power-up instruction, outputting the first clock signal as the processor clock signal in response to the outputted control signal from the decoder and a first clock wake-up end signal; and a first clock controller for, if the instruction is the power-down instruction, outputting the disable signal for disabling clock generation of the first clock generator in response to the control signal outputted from the decoder and the clock change end signal outputted from the clock selection unit and, if the instruction is the power-down instruction, outputting the enable signal for enabling the clock generation of the first clock generator in response to the control signal outputted from the decoder, and outputting the first wake-up end signal after a predetermined time.